

FIG.1

FIG. 2A is a block diagram of a system 100. The system 100 includes a plurality of processors 110₁, 110₂, ..., 110_N connected to a plurality of master buses 115₁, 115₂, ..., 115_N. Each master bus 115_i is connected to a master bus interface circuit 120. The master bus interface circuit 120 includes a bus controller 130_i and a data path 210. The data path 210 is connected to a slave device 140_{i1}, a slave device 140_{i2}, ..., a slave device 140_{iM}, and a slave device 140_{iL}. The slave devices 140_{i1}, 140_{i2}, ..., 140_{iM} are connected to a common memory interface 150, which is connected to a common memory 160.

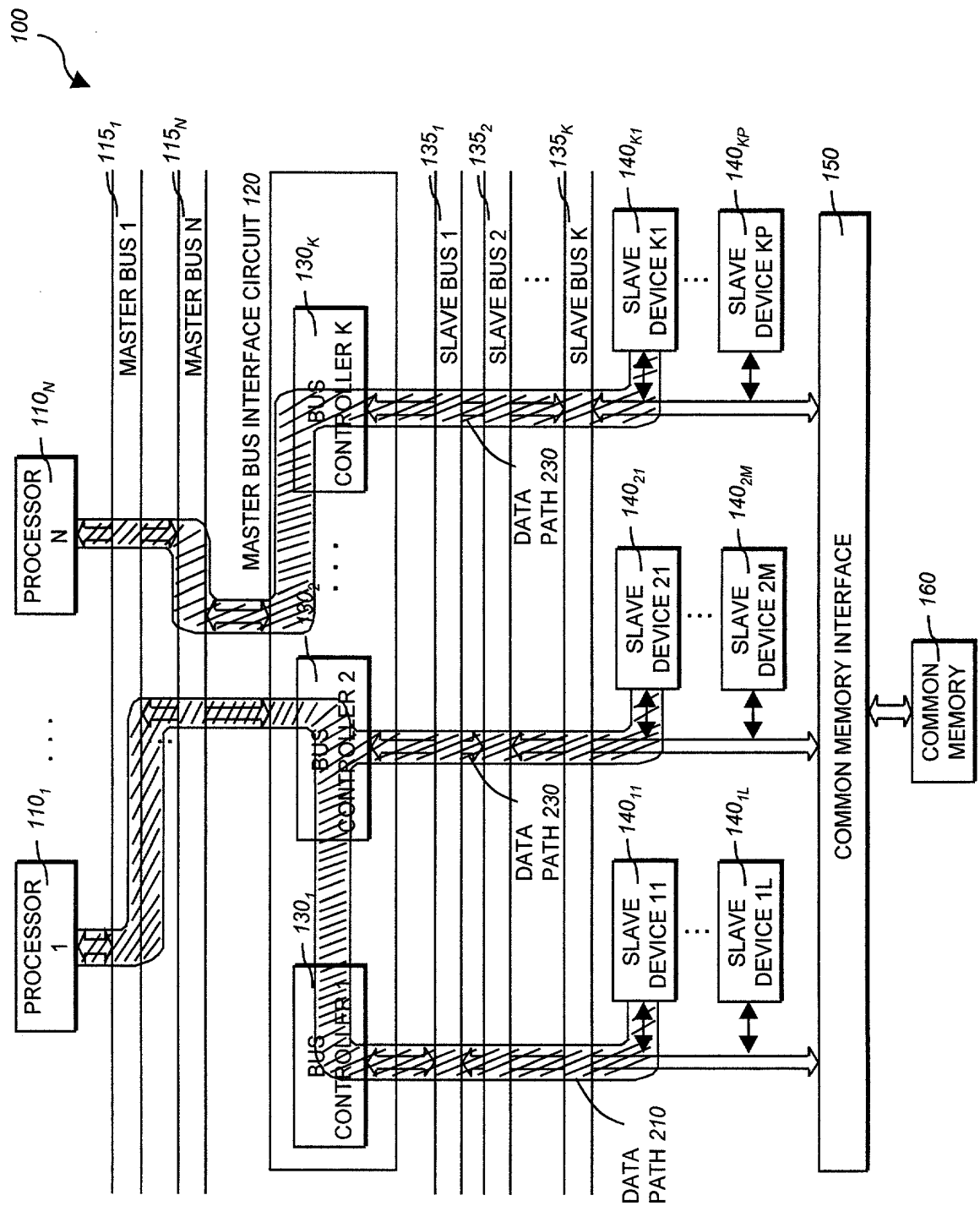


FIG. 2A

